REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-31 are pending in the present application. Claims 1, 4, 10, 14, and 16 are amended and Claim 31 is added by the present amendment.

In the outstanding Office Action, Claims 1, 9, 10, 14, and 15 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,380,569 to Chang et al. (herein "Chang") in view of U.S. Patent No. 5,998,833 to Baliga and U.S. Patent No. 6,285,060 to Korec et al. (herein "Korec") and U.S. Patent No. 6,525,375 to Yamaguchi et al. (herein "Yamaguchi") and U.S. Patent No. 5,828,101 to Endo; Claims 3, 5, 7, 11-13, 20, 21, 26, 27, and 30 were rejected under 35 U.S.C. § 103(a) as unpatentable over Chang in view of Baliga, Korec, U.S. Patent No. 5,831,288 to Singh et al. (herein "Singh"), Yamaguchi, and Endo; and Claims 2, 4, 6, 8, 16-19, 22-25, 28, and 29 were indicated as allowable if rewritten in independent form.

Applicants thank the Examiner for the indication of allowable subject matter.

Claims 1, 9, 10, 14, and 15 were rejected under 35 U.S.C. § 103(a) as unpatentable over Chang in view of Baliga, Korec, Yamaguchi, and Endo. That rejection is respectfully traversed.

Amended Claim 1 is directed to a power MOSFET including a lower resistive semi-conductor substrate of a first conductivity type, a drift layer of the first conductivity type, a high resistive epitaxial layer of the first conductivity type, trenches formed in the epitaxial layer and the drift layer, gate electrodes buried in the trenches with gate insulating films interposed between walls of the trenches and the gate electrodes, first and second low resistive source layers of the first conductivity type formed in a surface region of the epitaxial layer adjacent to the gate insulating films, a low resistive base layer of a second conductivity

type formed in the surface region of the epitaxial layer between the first and second source layers, a source electrode electrically and commonly connected to the source layers and the base layer, and a drain electrode electrically connected to the second main surface of the semi-conductor substrate. The drift layer has an impurity concentration higher than that of the epitaxial layer and the epitaxial layer intervening between the trenches is depleted in a case where no voltage is applied between the source electrode and the gate electrodes. Independent Claims 10 and 14 include similar features.

In a non-limiting example, FIG. 1 illustrates a trench and gate structure in which the n-- type base layer 3 is completely depleted when no voltage is applied between the source electrode 9 and the gate electrodes 6a and 6b (see page 10, lines 5-8). Furthermore, the n- drift layer 2 surrounds the bottom portions of the trenches 4a and 4b. In more detail, the power MOSFET of the claimed invention does not include P regions at the bottom regions of a pair of trenches 4a and 4b. In other words, the bottom portions of the trenches 4a and 4b are not surrounded by P regions but are surrounded by the n- type drift layer 2 having an impurity concentration higher than that of the base layer 3 as shown in FIG. 1. In an additional non-limiting example shown in FIGS. 4 and 5, the bottom portions of the trenches 4a, 4b and 24a, 24b are surrounded by n+ type substrate 1 and 21 having an impurity concentration higher than that of the base layer 3 and n- type drift layer 22, respectively.

In a further non-limiting example, FIG. 1 also illustrates a source electrode arrangement according to an embodiment of the claimed invention. As shown in FIG. 1, the upper portion of the n- base layer 3 is covered with the n+ source layers 7a and 7b and p+ base layer 8 provided between the n+ source layers 7a and 7b in one possible embodiment of the claimed invention. These n+ source layers 7a, 7b and the p+ base layer 8 are commonly connected to the source electrode 9. As shown in FIG. 8, the upper portion of the n- base layer 3 is covered with the n+ source layers 57a and 57b and p+ base layers 58a provided

between the n+ source layers 57a and 57b in one possible embodiment of the claimed invention. These n+ source layers 57a, 57b and p+ base layer 58a are commonly connected to the source electrode 63.

On the contrary, Chang shows in FIG. 1, for example, P regions 122 and 124 formed at the bottom regions of a pair of trenches 104 and 106. When no voltage is applied to the gate connection 134, the depletion region 140 is extended from the P regions 122 and 124 to form a potential barrier preventing the flow of current between the drain 130 and source 132 through the mesa region 108 in the N- drift layer 100. In the case of P- drift layer 400 shown in FIG. 5, N regions 222 and 224 form the depletion region in a similar manner.

Applicants respectfully submit that Chang also does not describe the claimed source electrode arrangement. According to FIG. 1 of Chang, for example, the upper portion of the N- drift layer 100 is completely covered with a single N+ ohmic contact layer 128 which is connected to the source electrode 128. In the case of P- drift layer 200 shown in FIG. 5, P+ ohmic contact layer 228 is provided. It is respectfully submitted Chang teaches no more than a single ohmic contact layer having the same conductivity type as that of the drift layer between the drift layer and the source electrode. Thus, Chang does not teach or suggest first and second low resistive source layers of the first conductivity type formed in a surface region of the epitaxial layer adjacent to the gate insulating films, a low resistive base layer of a second conductivity type formed in the surface region of the epitaxial layer between the first and second source layers, and a source electrode electrically and commonly connected to the source layers and the base layer, as in the claimed invention. Further, this feature of the claimed invention is not taught or suggested by Baliga, Korec, Yamaguchi, and Endo, either individually or in combination.

Accordingly, it is respectfully submitted independent Claims 1, 10 and 14, and each of the claims depending therefrom, are allowable.

Claims 3, 5, 7, 11-13, 20, 21, 26, 27 and 30 were rejected under 35 U.S.C. § 103(a) as unpatentable over Chang in view of Baliga, Korec, Singh, Yamaguchi, and Endo. That rejection is respectfully traversed.

Claims 3, 5, 7, 11-13, 20, 21, 26, 27 and 30 depend either directly or indirectly on independent Claims 1, 10, and 14, which as discussed above are believed to be allowable. Further, it is respectfully submitted that Baliga, Korec, Singh, Yamaguchi, and Endo also do not teach or suggest the features recited in the independent claims. Therefore, it is respectfully requested that rejection be withdrawn.

In addition, new Claim 31 is added to set forth the invention in a varying scope. In particular, new Claims 31 corresponds to the fourth embodiment shown in Figure 8. It is respectfully submitted the applied art does not teach or suggest the features recited in new Claim 31.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that affect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

David A. Bilodeau
Registration No. 42,325

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 08/03)

EHK:DAB:ZSS:dnf
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